MT6580 WCDMA Smartphone SoC Application Processor Technical Brief

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

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1 System Overview

MT6580 is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable 3G smart phone applications, with integrated Bluetooth, WiLAN, FM and GPS modules. Integrated RF solution offers exceptional radio performance under stringent ambient conditions. The chip integrates a Quad-core ARM® Cortex-A7 MPCore™ and supports various booting interfaces, including parallel NAND flash memory or eMMC, and 32-bit LPDDR2 or LPDDR3 for optimal performance, In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays, MMC/SD cards.

The application processor, a Quad-core ARM® Cortex-A7 MPCore™ offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also included to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders such as H.264 and MPEG-4. Audio supported includes FR, HR, EFR, AMR FR, and AMR HR vocoders, polyphonic ringtones and advanced audio functions such as echo cancellation, hands-free speakerphone operation and noise cancellation.

MT6580 provides feature-rich modem, capable of supporting Category 14 (21 Mbps) HSDPA downlink and Category 6 (5.76 Mbps) HSUPA uplink data rates, plus Class 12 GPRS and EDGE.

MT6580 also embodies wireless communication device, including WLAN, Bluetooth, FM and GPS. With four advanced radio technologies integrated into one single chip, MT6580 provides the best and most convenient connectivity solution among the industry. Advanced and sophisticated radio coexistence algorithms and hardware mechanisms are implemented with-in. It also supports single antenna sharing among 2.4 GHz antenna for Bluetooth, WLAN and 1.575 GHz for GPS.

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1.1 Platform Features

- **General**
  - Smartphone, 3 MCU subsystems architecture
  - eMMC & NAND boot support
  - Supports LPDDR2/LPDDR3
- **AP MCU subsystem**
  - Quad-core ARM® Cortex-A7 MPCore™
  - 1.3GHz clock rate
  - 32KB/32KB L1 I/D cache
  - 512KB unified L2 cache
- **MD external interfaces**
  - Supports dual SIM/USIM interface
  - Interface pins with RF peripherals (antenna tuner, PA, ...)
- **External memory interface**
  - Supports LPDDR/2/3, up to 2GB
  - 32-bit data bus width
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control
- **Peripherals**
  - USB2.0 HS/FS support
  - Supports NAND bootable, iNAND2® and MoviNAND®
  - 3 UART for debugging and applications
  - SPI master for external device
  - 3 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Maximum 5 PWM channels (depending on system configuration/IO usage)
  - I2S master output and master/slave input for connection with optional external hi-end audio codec
  - GPIOs
  - 2 sets of memory card controllers supporting SD/SDHC/MMC and SDIO protocols
- **Operating conditions**
  - Core DVFS voltage: 1.05~1.31v, sleep mode: 0.85v
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V
  - NAND: 1.8V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz
- **Package**
  - Type: TFBGA
  - 10.2mm x 11.0mm
  - Height: 1.1mm maximum
  - Ball count: 520 balls
  - Ball pitch: 0.4mm

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1.2 MODEM Feature

- **3G UMTS supported features**
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH
  - MAC-ehs
  - Uplink Cat.6, throughput up to 5.7Mbps
  - Downlink Cat. 14, throughput up to 21Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancement

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength (shared by 2G & 3G modem)
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - Two programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (single antenna interference cancellation) technology
  - Supports VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

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1.3 Cellular RF Features

- **General**
  - 26MHz internal DCXO
  - Supports GPS co-clock and 32kHz removal
  - RF calibration schemes for key RX and TX impairments
  - Low supply current & operation directly from DC-DC converter

- **Receiver**
  - Supports SAW-less GGE

- **Transmitter**
  - Polar (EPSK)/TPM (GMSK)
  - No external SAW filters required for TX
  - Single ADPLL synthesizer with fast settling

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1.4 Connectivity Features

- **Supports integrated Wi-Fi/BlueTooth/GPS**
  - Supports single antenna for Bluetooth and WLAN, GPS
  - Self calibration
  - Supports TCXO & TSX
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (for example, transmit window and duration that take into account protocol exchange sequence, frequency, etc.)

- **Wi-Fi**
  - Single-band (2.4GHz) single stream 802.11 b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (Hardware)
  - QoS: WFA WMM, WMM PS
  - Supports 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard)
  - Supports HotSpot 2.0 Passpoint
  - Per packet TX power control

- **BlueTooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Rx sensitivity: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality
  - Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - Supports GPS (WAAS/MSAS/EGNOS/GAGAN)
  - Best-in-class sensitivity performance
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 8 in-band tones
  - Low-power operational modes
  - Support TCXO
  - Support co-clock with AP/MD
  - 5Hz update rate
  - Supports external LNA

- **FM**
  - 65-108MHz worldwide FM bands with 50kHz tuning step
  - Supports RDS/RBDS radio data system
  - Digital stereo demodulator
  - Adaptive FM demodulator for both high and low-quality scenarios
  - Low sensitivity level with superior interference rejection
  - Programmable de-emphasis (b
  - Stereophonic multiplex signal (MPX)
  - signal detection and demodulation
  - Superior stereo noise reduction and soft mute volume control
  - Audio dynamic range control
  - Mono/stereo blending
  - Audio sensitivity3dBµVemf (SINAD=26dB)

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- Audio SINAD ≥ 60dB
- Supports Anti-jamming algorithm
- Supports short antenna

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1.5 Multimedia Features

- **Display**
  - Supports landscape or portrait panel resolution up to HD (1280x720)
  - MIPI DSI interface (3 data lanes)
  - Embedded LCD gamma correction
  - Supports true colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Supports spatial and temporal dithering
  - Supports side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Supports color enhancement
  - Supports adaptive contrast enhancement
  - Supports image/video/graphic sharpness enhancement
  - Supports dynamic backlight scaling

- **Graphics**
  - OpenGL ES 1.1/2.0 3D graphic accelerator capable of processing 53.25M tri/sec and 1000M pixel/sec @ 500MHz
  - OpenVG1.1 vector graphics accelerator

- **Image**
  - Supports 8 MP image capture
  - Supports camera raw sensor
  - Supports MIPI CSI-2 high-speed camera serial interface with 4 data lane (for main) + 2 data lane (for sub)

- **Video**
  - H.264 video encoder (720p) and decoder (1080p)
  - MPEG-4 video encoder (1080p) and decoder (1080p)

- **Audio**
  - Sampling rates supported: 8kHz to 48kHz
  - Sample formats supported: 8-bit/16-bit, Mono/Stereo

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR)
  - CTM
  - Dual-MIC input (A-MIC 16K in-band performance guarantee)
  - Digital MIC input (D-MIC hardware path supports 8K/16K/32K sample rate)

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1.6 General Description

MediaTek MT6580 is a highly integrated 3G System-on-chip (SoC) which incorporates advanced features, e.g. Quad-core ARM® Cortex-A7 MPCore™, 3D graphics (OpenGL|ES 2.0), 8M camera, high-definition 1080p video decoder, and built-in RF transceiver for multi-band GSM, GPRS, EDGE and W-CDMA cellular systems. MT6580 helps phone manufacturers build high-performance 3G smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

The World-leading Technology!

Based on MediaTek's world-leading mobile chip SoC architecture with advanced fab process, MT6580 is the brand-new generation smart phone SoC integrating MediaTek W-CDMA modem, Quad-core ARM® Cortex-A7 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in Features, High-valued Product!

To enrich the camera features, MT6580 equips a 8M camera with advanced features, e.g. auto focus, anti-handshake, auto sensor defect pixel correction, continuous video AF, face detection, burst shot, digital zoom and panorama view.

Incredible Browser Experience!

The Quad-core ARM® Cortex-A7 MPCore™ brings PC-like browser experiences and helps accelerate OpenGL|ES 2.0 3D Adobe Flash 10 rendering performance to an unbeatable level.

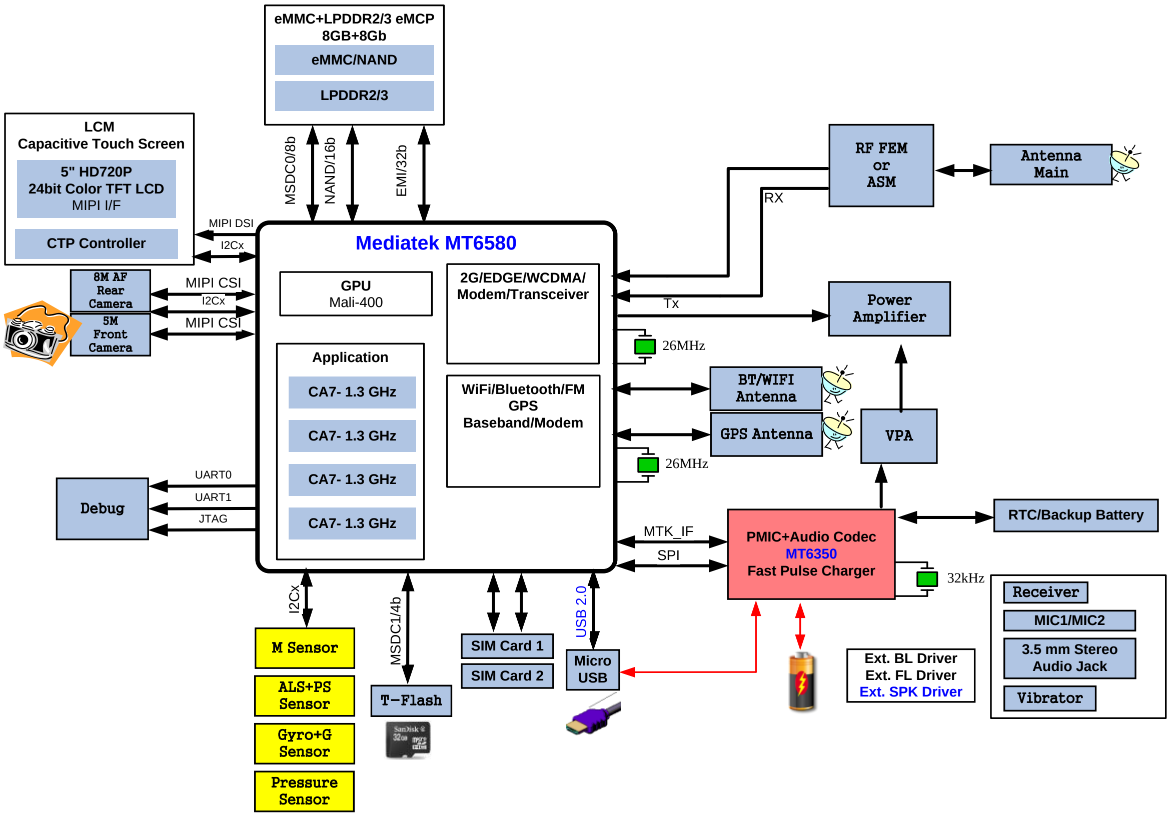

Figure 1-1. Block diagram of MT6580

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

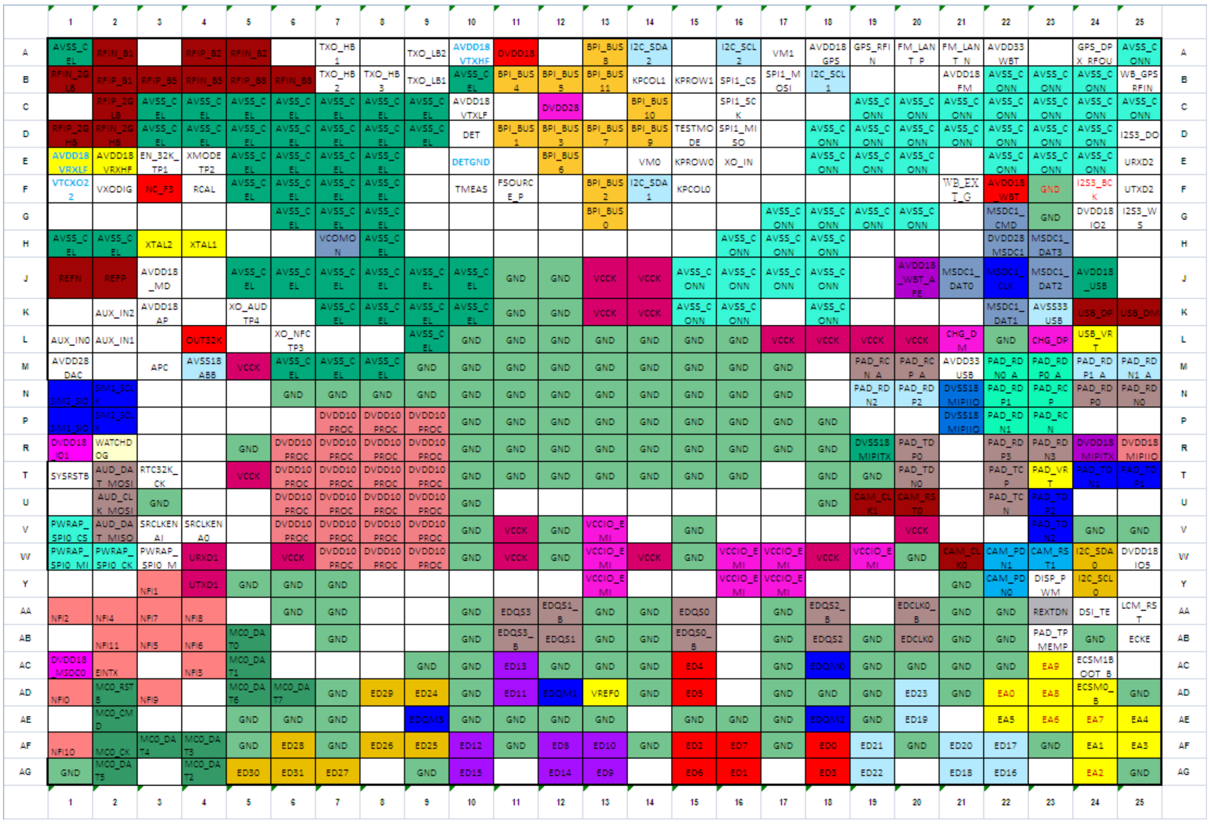

Figure 2-1. Ball map view for LPDDR2

2.1.2 Pin Coordinate

Table 2-1. Pin coordinate (use LPDDR2)

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	AVSS_CEL	B21	AVDD18_FM	L6	XO_NFC_TP3
A10	AVDD18_VTXHF	B22	AVSS_CONN	L9	AVSS_CEL
A11	DVDD18	B23	AVSS_CONN	M1	AVDD28_DAC
A13	BPI_BUS8	B24	AVSS_CONN	M10	GND
A14	I2C_SDA2	B25	WB_GPS_RFIN	M11	GND
A16	I2C_SCL2	B3	RFIP_B5	M12	GND
A17	VM1	B4	RFIN_B5	M13	GND
A18	AVDD18_GPS	B5	RFIP_B8	M14	GND

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A19	GPS_RFIN	B6	RFIN_B8	M15	GND
A2	RFIN_B1	B7	TXO_HB2	M16	GND
A20	FM_LANT_P	B8	TXO_HB3	M17	GND
A21	FM_LANT_N	B9	TXO_LB1	M19	PAD_RCN_A
A22	AVDD33_WBT	C10	AVDD18_VTXLF	M20	PAD_RCP_A
A24	GPS_DPX_RFOUT	C12	DVDD28	M21	AVDD33_USB
A25	AVSS_CONN	C14	BPI_BUS10	M22	PAD_RDN0_A
A4	RFIP_B2	C16	SPI1_SCK	M23	PAD_RDP0_A
A5	RFIN_B2	C19	AVSS_CONN	M24	PAD_RDP1_A
A7	TXO_HB1	C2	RFIP_2GLB	M25	PAD_RDN1_A
A9	TXO_LB2	C20	AVSS_CONN	M3	APC
AA1	NFI2	C21	AVSS_CONN	M4	AVSS18_ABB
AA10	GND	C22	AVSS_CONN	M5	VCCK
AA11	EDQS3	C23	AVSS_CONN	M6	AVSS_CEL
AA12	EDQS1_B	C24	AVSS_CONN	M7	AVSS_CEL
AA13	GND	C25	AVSS_CONN	M8	AVSS_CEL
AA14	GND	C3	AVSS_CEL	M9	GND
AA15	EDQS0	C4	AVSS_CEL	N1	SIM2_SIO
AA17	GND	C5	AVSS_CEL	N10	GND
AA18	EDQS2_B	C6	AVSS_CEL	N11	GND
AA2	NFI4	C7	AVSS_CEL	N12	GND
AA20	EDCLK0_B	C8	AVSS_CEL	N13	GND
AA21	GND	C9	AVSS_CEL	N14	GND
AA22	GND	D1	RFIP_2GHB	N15	GND
AA23	REXTDN	D10	DET	N16	GND
AA24	DSI_TE	D11	BPI_BUS1	N17	GND
AA25	LCM_RST	D12	BPI_BUS3	N19	PAD_RDN2
AA3	NFI7	D13	BPI_BUS7	N2	SIM1_SCLK
AA4	NFI8	D14	BPI_BUS9	N20	PAD_RDP2
AA6	GND	D15	TESTMODE	N21	DVSS18_MIPIIO
AA7	GND	D16	SPI1_MISO	N22	PAD_RDP1
AB10	GND	D18	AVSS_CONN	N23	PAD_RCP
AB11	EDQS3_B	D19	AVSS_CONN	N24	PAD_RDP0
AB12	EDQS1	D2	RFIN_2GHB	N25	PAD_RDN0
AB13	GND	D20	AVSS_CONN	N6	GND
AB14	GND	D21	AVSS_CONN	N7	GND
AB15	EDQS0_B	D22	AVSS_CONN	N8	GND
AB17	GND	D23	AVSS_CONN	N9	GND
AB18	EDQS2	D24	AVSS_CONN	P1	SIM1_SIO
AB19	GND	D25	I2S3_DO	P10	GND
AB2	NFI11	D3	AVSS_CEL	P11	GND
AB20	EDCLK0	D4	AVSS_CEL	P12	GND
AB21	GND	D5	AVSS_CEL	P13	GND
AB22	GND	D6	AVSS_CEL	P14	GND
AB23	PAD_TP_MEMPL L	D7	AVSS_CEL	P15	GND

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AB24	GND	D8	AVSS_CEL	P16	GND
AB25	ECKE	D9	AVSS_CEL	P17	GND
AB3	NFI5	E1	AVDD18_VRXLF	P18	GND
AB4	NFI6	E10	DETGND	P2	SIM2_SCLK
AB5	MC0_DAT0	E12	BPI_BUS6	P21	DVSS18_MIPIIO
AB7	GND	E14	VM0	P22	PAD_RDN1
AC1	DVDD18_MSDC0	E15	KPROW0	P23	PAD_RCN
AC10	GND	E16	XO_IN	P7	DVDD10_PROC
AC11	ED13	E18	AVSS_CONN	P8	DVDD10_PROC
AC12	GND	E19	AVSS_CONN	P9	DVDD10_PROC
AC13	GND	E2	AVDD18_VRXHF	R1	DVDD18_IO1
AC14	GND	E20	AVSS_CONN	R10	GND
AC15	ED4	E22	AVSS_CONN	R11	GND
AC17	GND	E23	AVSS_CONN	R12	GND
AC18	EDQM0	E24	AVSS_CONN	R13	GND
AC19	GND	E25	URXD2	R14	GND
AC2	EINTX	E3	EN_32K_TP1	R15	GND
AC20	GND	E4	XMODE_TP2	R16	GND
AC21	GND	E5	AVSS_CEL	R17	GND
AC22	GND	E6	AVSS_CEL	R18	GND
AC23	EA9	E7	AVSS_CEL	R19	DVSS18_MIPITX
AC24	ECSM1BOOT_B	E8	AVSS_CEL	R2	WATCHDOG
AC4	NFI3	F1	VTCXO22	R20	PAD_TDP0
AC5	MC0_DAT1	F10	TMEAS	R22	PAD_RDP3
AC9	GND	F11	FSOURCE_P	R23	PAD_RDN3
AD1	NFI0	F13	BPI_BUS2	R24	DVDD18_MIPITX
AD10	GND	F14	I2C_SDA1	R25	DVDD18_MIPIIO
AD11	ED11	F15	KPCOL0	R5	GND
AD12	EDQM1	F2	VXODIG	R6	DVDD10_PROC
AD13	VREF0	F21	WB_EXT_G	R7	DVDD10_PROC
AD14	GND	F22	AVDD18_WBT	R8	DVDD10_PROC
AD15	ED5	F23	GND	R9	DVDD10_PROC
AD17	GND	F24	I2S3_BCK	T1	SYSRSTB
AD18	GND	F25	UTXD2	T10	GND
AD19	GND	F3	NC_F3	T11	GND
AD2	MC0_RSTB	F4	RCAL	T12	GND
AD20	ED23	F5	AVSS_CEL	T13	GND
AD21	GND	F6	AVSS_CEL	T14	GND
AD22	EA0	F7	AVSS_CEL	T15	GND
AD23	EA8	F8	AVSS_CEL	T16	GND
AD24	ECSM0_B	G13	BPI_BUS0	T18	GND
AD25	GND	G17	AVSS_CONN	T19	GND
AD3	NFI9	G18	AVSS_CONN	T2	AUD_DAT_MOSI
AD5	MC0_DAT6	G19	AVSS_CONN	T20	PAD_TDN0
AD6	MC0_DAT7	G20	AVSS_CONN	T22	PAD_TCP
AD7	GND	G22	MSDC1_CMD	T23	PAD_VRT

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AD8	ED29	G23	GND	T24	PAD_TDN1
AD9	ED24	G24	DVDD18_IO2	T25	PAD_TDP1
AE10	GND	G25	I2S3_WS	T3	RTC32K_CK
AE11	GND	G6	AVSS_CEL	T5	VCCK
AE12	GND	G7	AVSS_CEL	T6	DVDD10_PROC
AE13	GND	G8	AVSS_CEL	T7	DVDD10_PROC
AE15	GND	H1	AVSS_CEL	T8	DVDD10_PROC
AE16	GND	H16	AVSS_CONN	T9	DVDD10_PROC
AE17	GND	H17	AVSS_CONN	U10	GND
AE18	EDQM2	H18	AVSS_CONN	U18	GND
AE19	GND	H2	AVSS_CEL	U19	CAM_CLK1
AE2	MC0_CMD	H22	DVDD28_MSDC1	U2	AUD_CLK_MOSI
AE20	ED19	H23	MSDC1_DAT3	U20	CAM_RST0
AE22	EA5	H3	XTAL2	U22	PAD_TCN
AE23	EA6	H4	XTAL1	U23	PAD_TDP2
AE24	EA7	H7	VCOMON	U3	GND
AE25	EA4	H8	AVSS_CEL	U6	DVDD10_PROC
AE5	GND	J1	REFN	U7	DVDD10_PROC
AE6	GND	J10	AVSS_CEL	U8	DVDD10_PROC
AE7	GND	J11	GND	U9	DVDD10_PROC
AE9	EDQM3	J12	GND	V1	PWRAP_SPI0_CS N
AF1	NFI10	J13	VCCK	V10	GND
AF10	ED12	J14	VCCK	V11	VCCK
AF11	GND	J15	AVSS_CONN	V12	GND
AF12	ED8	J16	AVSS_CONN	V13	VCCIO_EMI
AF13	ED10	J17	AVSS_CONN	V15	GND
AF14	GND	J18	AVSS_CONN	V2	AUD_DAT_MISO
AF15	ED2	J2	REFP	V20	VCCK
AF16	ED7	J20	AVDD18_WBT_AFE	V23	PAD_TDN2
AF17	GND	J21	MSDC1_DAT0	V24	GND
AF18	ED0	J22	MSDC1_CLK	V25	GND
AF19	ED21	J23	MSDC1_DAT2	V3	SRCLKENAI
AF2	MC0_CK	J24	AVDD18_USB	V4	SRCLKENA0
AF20	GND	J3	AVDD18_MD	V6	DVDD10_PROC
AF21	ED20	J5	AVSS_CEL	V7	DVDD10_PROC
AF22	ED17	J6	AVSS_CEL	V8	DVDD10_PROC
AF23	GND	J7	AVSS_CEL	V9	DVDD10_PROC
AF24	EA1	J8	AVSS_CEL	W1	PWRAP_SPI0_MI
AF25	EA3	J9	AVSS_CEL	W10	GND
AF3	MC0_DAT4	K10	AVSS_CEL	W11	VCCK
AF4	MC0_DAT3	K11	GND	W12	GND
AF5	GND	K12	GND	W13	VCCIO_EMI
AF6	ED28	K13	VCCK	W14	VCCK
AF7	GND	K14	VCCK	W15	GND
AF8	ED26	K15	AVSS_CONN	W16	VCCIO_EMI

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AF9	ED25	K16	AVSS_CONN	W17	VCCIO_EMI
AG1	GND	K18	AVSS_CONN	W18	VCCK
AG10	ED15	K2	AUX_IN2	W19	VCCIO_EMI
AG12	ED14	K22	MSDC1_DAT1	W2	PWRAP_SPI0_CK
AG13	ED9	K23	AVSS33_USB	W20	GND
AG15	ED6	K24	USB_DP	W21	CAM_CLK0
AG16	ED1	K25	USB_DM	W22	CAM_PDN1
AG18	ED3	K3	AVDD18_AP	W23	CAM_RST1
AG19	ED22	K5	XO_AUD_TP4	W24	I2C_SDA0
AG2	MC0_DAT5	K7	AVSS_CEL	W25	DVDD18_IO5
AG21	ED18	K8	AVSS_CEL	W3	PWRAP_SPI0_MO
AG22	ED16	K9	AVSS_CEL	W4	URXD1
AG24	EA2	L1	AUX_IN0	W6	VCCK
AG25	GND	L10	GND	W7	DVDD10_PROC
AG4	MC0_DAT2	L11	GND	W8	DVDD10_PROC
AG5	ED30	L12	GND	W9	DVDD10_PROC
AG6	ED31	L13	GND	Y13	VCCIO_EMI
AG7	ED27	L14	GND	Y16	VCCIO_EMI
AG9	GND	L15	GND	Y17	VCCIO_EMI
B1	RFIN_2GLB	L16	GND	Y21	GND
B10	AVSS_CEL	L17	VCCK	Y22	CAM_PDN0
B11	BPI_BUS4	L18	VCCK	Y23	DISP_PWM
B12	BPI_BUS5	L19	VCCK	Y24	I2C_SCL0
B13	BPI_BUS11	L2	AUX_IN1	Y3	NFI1
B14	KPCOL1	L20	VCCK	Y4	UTXD1
B15	KPROW1	L21	CHG_DM	Y5	GND
B16	SPI1_CS	L22	GND	Y6	GND
B17	SPI1_MOSI	L23	CHG_DP	Y7	GND
B18	I2C_SCL1	L24	USB_VRT		
B2	RFIP_B1	L4	OUT32K		

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

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Table 2-3. Detailed pin description (using LPDDR2)

Ball name	Type	Description	Power domain
System			
SRCLKENA0	DIO	26MHz clock enable output	DVDD18_IO1
SRCLKENAI	DIO	I: 26MHz clock enable input	DVDD18_IO1
SYSRSTB	DI	System reset input	DVDD18_IO1
TESTMODE	DI	Test mode	DVDD18
WATCHDOG	DIO	Watchdog reset output	DVDD18_IO1
RTC32K_CK	DI	32K clock input	DVDD18_IO1
PMIC			
PWRAP_SPI0_CSN	DIO	PMIC interface - SPI control	DVDD18_IO1
PWRAP_SPI0_MI	DIO	PMIC interface - SPI control	DVDD18_IO1
PWRAP_SPI0_MO	DIO	PMIC interface - SPI control	DVDD18_IO1
PWRAP_SPI0_CK	DIO	PMIC interface - SPI control	DVDD18_IO1
AUD_CLK_MOSI	DIO	PMIC interface - Audio	DVDD18_IO1
AUD_DAT_MISO	DIO	PMIC interface - Audio	DVDD18_IO1
AUD_DAT_MOSI	DIO	PMIC interface - Audio	DVDD18_IO1
EINTX	DIO	PMIC interface - Interrupt	DVDD18_MSDC0
SIM1_SCLK	DIO	PMIC interface - SIM1 clock	DVDD18_IO1
SIM1_SIO	DIO	PMIC interface - SIM1 data	DVDD18_IO1
SIM2_SCLK	DIO	PMIC interface - SIM2 clock	DVDD18_IO1
SIM2_SIO	DIO	PMIC interface - SIM2 data	DVDD18_IO1
Display			
DISP_PWM	DIO	LCM black light control (dimming/CABC)	DVDD18_IO5
DSI_TE	DIO	Tearing free	DVDD18_IO5
LCM_RST	DIO	Display reset	DVDD18_IO5
MIPI DSI			
PAD_VRT	AIO	MIPI DSI bias pin; connects 1.5Kohm 1% resistor to ground	DVDD18_MIPITX
PAD_TCP	AIO	MIPI DSI0 Clock Lane positive	DVDD18_MIPITX
PAD_TCN	AIO	MIPI DSI0 Clock lane negative	DVDD18_MIPITX
PAD_TDP0	AIO	MIPI DSI0 Data Lane0 positive	DVDD18_MIPITX
PAD_TDN0	AIO	MIPI DSI0 Data Lane0 negative	DVDD18_MIPITX
PAD_TDP1	AIO	MIPI DSI0 Data Lane1 positive	DVDD18_MIPITX
PAD_TDN1	AIO	MIPI DSI0 Data Lane1 negative	DVDD18_MIPITX
PAD_TDP2	AIO	MIPI DSI0 Data Lane2 positive	DVDD18_MIPITX
PAD_TDN2	AIO	MIPI DSI0 Data Lane2 negative	DVDD18_MIPITX
Camera			
CAM_CLK0	DIO	Camera interface – CLK 0	DVDD18_IO5
CAM_CLK1	DIO	Camera interface – CLK 1	DVDD18_IO5
CAM_PDN0	DIO	Camera interface - Power down 0	DVDD18_IO5
CAM_PDN1	DIO	Camera interface - Power down 1	DVDD18_IO5
CAM_RST0	DIO	Camera interface – Reset 0	DVDD18_IO5

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Ball name	Type	Description	Power domain
CAM_RST1	DIO	Camera interface – Reset 1	DVDD18_IO5
MIPI CSI0 & CSI1			
PAD_RCP	AIO	MIPI CSI0 Clock Lane positive	DVDD18_MIPIIO
PAD_RCN	AIO	MIPI CSI0 Clock lane negative	DVDD18_MIPIIO
PAD_RDP0	AIO	MIPI CSI0 Data Lane0 positive	DVDD18_MIPIIO
PAD_RDN0	AIO	MIPI CSI0 Data Lane0 negative	DVDD18_MIPIIO
PAD_RDP1	AIO	MIPI CSI0 Data Lane1 positive	DVDD18_MIPIIO
PAD_RDN1	AIO	MIPI CSI0 Data Lane1 negative	DVDD18_MIPIIO
PAD_RDP2	AIO	MIPI CSI0 Data Lane2 positive	DVDD18_MIPIIO
PAD_RDN2	AIO	MIPI CSI0 Data Lane2 negative	DVDD18_MIPIIO
PAD_RDP3	AIO	MIPI CSI0 Data Lane3 positive	DVDD18_MIPIIO
PAD_RDN3	AIO	MIPI CSI0 Data Lane3 negative	DVDD18_MIPIIO
PAD_RCP_A	AIO	MIPI CSI1 Clock Lane positive	DVDD18_MIPIIO
PAD_RCN_A	AIO	MIPI CSI1 Clock Lane negative	DVDD18_MIPIIO
PAD_RDP0_A	AIO	MIPI CSI1 Data Lane0 positive	DVDD18_MIPIIO
PAD_RDN0_A	AIO	MIPI CSI1 Data Lane0 negative	DVDD18_MIPIIO
PAD_RDP1_A	AIO	MIPI CSI1 Data Lane1 positive	DVDD18_MIPIIO
PAD_RDN1_A	AIO	MIPI CSI1 Data Lane1 negative	DVDD18_MIPIIO
USB			
USB_DM	AIO	USB D- differential data line	AVDD33_USB
USB_DP	AIO	USB D+ differential data line	AVDD33_USB
USB_VRT	AIO	USB bias pin; connects 5.11Kohm 1% resistor to ground	AVDD18_USB
CHG_DM	AIO	BC 1.1 charger DP from PMIC	AVDD33_USB
CHG_DP	AIO	BC 1.1 charger DM from PMIC	AVDD33_USB
ABB			
AUX_IN2	AI	AUXADC external input channel 2	AVDD18_AP
AUX_IN1	AI	AUXADC external input channel 1	AVDD18_AP
AUX_IN0	AI	AUXADC external input channel 0	AVDD18_AP
APC	AO	Automatic power control for CellRF power amplifier	AVDD28_DAC
REFN	G	Negative reference port for internal circuit	AVDD18_AP
REFP	AO	Positive reference port for internal circuit	AVDD18_AP
MEMPLL – Analog			
PAD_TP_MEMPLL	AO	Test pin	DVDD18_MIPITX
Cellular RF – RF			
XTAL1	AI	CellRF XO input	VTCXO22
XTAL2	AI	CellRF XO input	VTCXO22
TXO_HB1	AO	CellRF 2G HB TX output	VRF18
TXO_HB2	AO	CellRF 3G HB TX output 1	VRF18
TXO_HB3	AO	CellRF 3G HB TX output 2	VRF18
TXO_LB1	AO	CellRF 3G LB TX output	VRF18
TXO_LB2	AO	CellRF 2G LB TX output	VRF18
XO_NFC_TP3	AO	Sine-26MHz output clock (ATV/NFC)/test pin 3	VTCXO22

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Ball name	Type	Description	Power domain
XO_AUD_TP4	AO	26MHz output clock (PMIC/Audio)/test pin 4	VTCXO22
OUT32K	AO	32KHz clock output	VTCXO22
EN_32K_TP1	DI/AO	32KHz function enable (with 32kHz XO, EN=0; without 32kHz XO, EN=1)/test pin 1	VTCXO22
XMODE_TP2	DI/AO	DCXO(=1)/VCTCXO(=0) selection/test pin2	VTCXO22
RFIN_2GLB	AI	CellRF 2G LB RX input	VRF18
RFIP_2GLB	AI	CellRF 2G LB RX input	VRF18
RFIN_2GHB	AI	CellRF 2G HB RX input	VRF18
RFIP_2GHB	AI	CellRF 2G HB RX input	VRF18
VCOMON	AO	CellRF Monitor port for RFVCO	VRF18
RCAL	AIO	R calibration ext resistor connection	VRF18
DET	AI	CellRF TX detection path input	VRF18
TMEAS	AI	External temperature measurement input	VRF18
RFIN_B8	AI	CellRF Band 8 RX input	VRF18
RFIP_B8	AI	CellRF Band 8 RX input	VRF18
RFIN_B5	AI	CellRF Band 5 RX input	VRF18
RFIP_B5	AI	CellRF Band 5 RX input	VRF18
RFIN_B2	AI	CellRF Band 2 RX input	VRF18
RFIP_B2	AI	CellRF Band 2 RX input	VRF18
RFIN_B1	AI	CellRF Band 1 RX input	VRF18
RFIP_B1	AI	CellRF Band 1 RX input	VRF18
Baseband Parallel Interface			
BPI_BUS0	DIO	Baseband parallel interface data 0 (2.8V)	DVDD28
BPI_BUS1	DIO	Baseband parallel interface data 1 (2.8V)	DVDD28
BPI_BUS2	DIO	Baseband parallel interface data 2 (2.8V)	DVDD28
BPI_BUS3	DIO	Baseband parallel interface data 3 (2.8V)	DVDD28
BPI_BUS4	DIO	Baseband parallel interface data 4 (1.8V)	DVDD18
BPI_BUS5	DIO	Baseband parallel interface data 5 (1.8V)	DVDD18
BPI_BUS6	DIO	Baseband parallel interface data 6 (1.8V)	DVDD18
BPI_BUS7	DIO	Baseband parallel interface data 7 (1.8V)	DVDD18
BPI_BUS8	DIO	Baseband parallel interface data 8 (1.8V)	DVDD18
BPI_BUS9	DIO	Baseband parallel interface data 9 (1.8V)	DVDD18
BPI_BUS10	DIO	Baseband parallel interface data 10 (1.8V)	DVDD18
BPI_BUS11	DIO	Baseband parallel interface data 11 (1.8V)	DVDD18
VM0	DIO	PA mode selection (1.8V)	DVDD18
VM1	DIO	PA mode selection (1.8V)	DVDD18
Connectivity Interface -- Analog			
WB_EXT_G	AI	Aux LNA input	AVDD18_WBT
XO_IN	AI	Dedicated 26MHz clock (TCXO option) for connectivity system	AVDD18_GPS
GPS_DPX_RFOUT	AO	Default is NC (option for w/o GPS eLNA solution)	AVDD33_WBT
WB_GPS_RFIN	AIO	Default is for WF/BT RF I/O port.	AVDD33_WBT
FM_LANT_N	G	Connect to GND	AVDD18_FM

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Ball name	Type	Description	Power domain
FM_LANT_P	AI	FM receiver RF input	AVDD18_FM
GPS_RFIN	AI	GPS receiver RF input	AVDD18_GPS
DRAM Interface			
VREF0	DIO	VREF for DRAM IO	VCCIO_EMI
EDCLK0	DIO	DRAM clock 0 pin positive	VCCIO_EMI
EDCLK0_B	DIO	DRAM clock 0 pin negative	VCCIO_EMI
ECKE	DIO	DRAM command address - CKE	VCCIO_EMI
ECSM0_B	DIO	DRAM command address - CS0	VCCIO_EMI
ECSM1BOOT_B	DIO	DRAM command address - CS1	VCCIO_EMI
REXTDN	DIO	DRAM IO driving calibration Resistor	VCCIO_EMI
EA0	DIO	DRAM command address - A0	VCCIO_EMI
EA1	DIO	DRAM command address - A1	VCCIO_EMI
EA2	DIO	DRAM command address - A2	VCCIO_EMI
EA3	DIO	DRAM command address - A3	VCCIO_EMI
EA4	DIO	DRAM command address - A4	VCCIO_EMI
EA5	DIO	DRAM command address - A5	VCCIO_EMI
EA6	DIO	DRAM command address - A6	VCCIO_EMI
EA7	DIO	DRAM command address - A7	VCCIO_EMI
EA8	DIO	DRAM command address - A8	VCCIO_EMI
EA9	DIO	DRAM command address - A9	VCCIO_EMI
ED0	DIO	DRAM data 0	VCCIO_EMI
ED1	DIO	DRAM data 1	VCCIO_EMI
ED2	DIO	DRAM data 2	VCCIO_EMI
ED3	DIO	DRAM data 3	VCCIO_EMI
ED4	DIO	DRAM data 4	VCCIO_EMI
ED5	DIO	DRAM data 5	VCCIO_EMI
ED6	DIO	DRAM data 6	VCCIO_EMI
ED7	DIO	DRAM data 7	VCCIO_EMI
ED8	DIO	DRAM data 8	VCCIO_EMI
ED9	DIO	DRAM data 9	VCCIO_EMI
ED10	DIO	DRAM data 10	VCCIO_EMI
ED11	DIO	DRAM data 11	VCCIO_EMI
ED12	DIO	DRAM data 12	VCCIO_EMI
ED13	DIO	DRAM data 13	VCCIO_EMI
ED14	DIO	DRAM data 14	VCCIO_EMI
ED15	DIO	DRAM data 15	VCCIO_EMI
ED16	DIO	DRAM data 16	VCCIO_EMI
ED17	DIO	DRAM data 17	VCCIO_EMI
ED18	DIO	DRAM data 18	VCCIO_EMI
ED19	DIO	DRAM data 19	VCCIO_EMI
ED20	DIO	DRAM data 20	VCCIO_EMI
ED21	DIO	DRAM data 21	VCCIO_EMI

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Ball name	Type	Description	Power domain
ED22	DIO	DRAM data 22	VCCIO_EMI
ED23	DIO	DRAM data 23	VCCIO_EMI
ED24	DIO	DRAM data 24	VCCIO_EMI
ED25	DIO	DRAM data 25	VCCIO_EMI
ED26	DIO	DRAM data 26	VCCIO_EMI
ED27	DIO	DRAM data 27	VCCIO_EMI
ED28	DIO	DRAM data 28	VCCIO_EMI
ED29	DIO	DRAM data 29	VCCIO_EMI
ED30	DIO	DRAM data 30	VCCIO_EMI
ED31	DIO	DRAM data 31	VCCIO_EMI
EDQM0	DIO	DRAM Data Mask 0	VCCIO_EMI
EDQM1	DIO	DRAM Data Mask 1	VCCIO_EMI
EDQM2	DIO	DRAM Data Mask 2	VCCIO_EMI
EDQM3	DIO	DRAM Data Mask 3	VCCIO_EMI
EDQS0	DIO	DRAM Data Strobe 0 positive	VCCIO_EMI
EDQS0_B	DIO	DRAM Data Strobe 0 negative	VCCIO_EMI
EDQS1	DIO	DRAM Data Strobe 1 positive	VCCIO_EMI
EDQS1_B	DIO	DRAM Data Strobe 1 negative	VCCIO_EMI
EDQS2	DIO	DRAM Data Strobe 2 positive	VCCIO_EMI
EDQS2_B	DIO	DRAM Data Strobe 2 negative	VCCIO_EMI
EDQS3	DIO	DRAM Data Strobe 3 positive	VCCIO_EMI
EDQS3_B	DIO	DRAM Data Strobe 3 negative	VCCIO_EMI
MSDC 0 (eMMC)			
MC0_CK	DIO	MSDC0 interface - Clock	DVDD18_MSDC0
MC0_CMD	DIO	MSDC0 interface - Command	DVDD18_MSDC0
MC0_DAT0	DIO	MSDC0 interface - Data pin 0	DVDD18_MSDC0
MC0_DAT1	DIO	MSDC0 interface - Data pin 1	DVDD18_MSDC0
MC0_DAT2	DIO	MSDC0 interface - Data pin 2	DVDD18_MSDC0
MC0_DAT3	DIO	MSDC0 interface - Data pin 3	DVDD18_MSDC0
MC0_DAT4	DIO	MSDC0 interface - Data pin 4	DVDD18_MSDC0
MC0_DAT5	DIO	MSDC0 interface - Data pin 5	DVDD18_MSDC0
MC0_DAT6	DIO	MSDC0 interface - Data pin 6	DVDD18_MSDC0
MC0_DAT7	DIO	MSDC0 interface - Data pin 7	DVDD18_MSDC0
MC0_RSTB	DIO	MSDC0 interface - Reset	DVDD18_MSDC0
NAND Flash Interface			
NFI0	DIO	NAND flash interface pin 0 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI1	DIO	NAND flash interface pin 1 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI2	DIO	NAND flash interface pin 2 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI3	DIO	NAND flash interface pin 3 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI4	DIO	NAND flash interface pin 4 (see pin mux for detailed	DVDD18_MSDC0

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Ball name	Type	Description	Power domain
		mapping)	
NFI5	DIO	NAND flash interface pin 5 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI6	DIO	NAND flash interface pin 6 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI7	DIO	NAND flash interface pin 7 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI8	DIO	NAND flash interface pin 8 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI9	DIO	NAND flash interface pin 9 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI10	DIO	NAND flash interface pin 10 (see pin mux for detailed mapping)	DVDD18_MSDC0
NFI11	DIO	NAND flash interface pin 11 (see pin mux for detailed mapping)	DVDD18_MSDC0
MSDC 1 (SD Card)			
MSDC1_CLK	DIO	MSDC1 interface - Clock	DVDD28_MSDC1
MSDC1_CMD	DIO	MSDC1 interface - Command	DVDD28_MSDC1
MSDC1_DAT0	DIO	MSDC1 interface - Data pin 0	DVDD28_MSDC1
MSDC1_DAT1	DIO	MSDC1 interface - Data pin 1	DVDD28_MSDC1
MSDC1_DAT2	DIO	MSDC1 interface - Data pin 2	DVDD28_MSDC1
MSDC1_DAT3	DIO	MSDC1 interface - Data pin 3	DVDD28_MSDC1
Keypad Interface			
KPCOL0	DIO	Keypad column 0	DVDD18
KPCOL1	DIO	Keypad column 1	DVDD18
KPROW0	DIO	Keypad row 0	DVDD18
KPROW1	DIO	Keypad row 1	DVDD18
I2C			
I2C_SCL0	DIO	I2C 0 clock	DVDD18_IO5
I2C_SDA0	DIO	I2C 0 data	DVDD18_IO5
I2C_SCL1	DIO	I2C 1 clock	DVDD18
I2C_SDA1	DIO	I2C 1 data	DVDD18
I2C_SCL2	DIO	I2C 2 clock	DVDD18
I2C_SDA2	DIO	I2C 2 data	DVDD18
UART			
URXD1	DIO	UART1 RX	DVDD18_MSDC0
UTXD1	DIO	UART1 TX	DVDD18_MSDC0
URXD2	DIO	UART2 RX	DVDD18_IO2
UTXD2	DIO	UART2 TX	DVDD18_IO2
SPI			
SPI1_CS	DIO	SPI chip select	DVDD18
SPI1_MISO	DIO	SPI data in (master in, slave out)	DVDD18
SPI1_MOSI	DIO	SPI data out (master out, slave in)	DVDD18
SPI1_SCK	DIO	SPI clock	DVDD18
I2S			

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Ball name	Type	Description	Power domain
I2S3_DO	DIO	I2S data output	DVDD18_IO2
I2S3_BCK	DIO	I2S bit clock	DVDD18_IO2
I2S3_WS	DIO	I2S word select	DVDD18_IO2
Analog Power			
DVDD18_MIPIIO	P	Analog power 1.8V for MIPI	DVDD18_MIPIIO
DVDD18_MIPITX	P	Analog power 1.8V for MIPI	DVDD18_MIPITX
AVDD18_USB	P	Analog power 1.8V for USB	AVDD18_USB
AVDD18_MD	P	Analog power input 1.8V for BBTX, BBRX, RF VIO	AVDD18_MD
AVDD18_AP	P	Analog power Input 1.8V for AUXADC, TSENSE	AVDD18_AP
AVDD28_DAC	P	Analog power input 2.8V for APC	AVDD28_DAC
AVDD33_USB	P	Analog power 3.3V for USB	AVDD33_USB
AVDD18_FM	P	Analog power 1.8V for FM	AVDD18_FM
AVDD18_GPS	P	Analog power 1.8V for GPS	AVDD18_GPS
AVDD18_WBT_AFE	P	Analog power 1.8V for WBT AFE	AVDD18_WBT_AFE
AVDD18_WBT	P	Analog power 1.8V for WBT	AVDD18_WBT
AVDD33_WBT	P	Analog power 3.3V for WBT	AVDD33_WBT
AVDD_VIO18	P	Analog power 1.8V for Cell RF ISO and LSFLDO (VIO18 from PMIC)	AVDD_VIO18
VXODIG	P	Cell RF 32k/32kless power domain switch (VIO18 or VTCXO22)	VXODIG
VTCXO22	P	Cell RF DCXO core/buffer power (VTCXO22 from PMIC)	VTCXO22
AVDD18_VRXLF	P	Cell RF RX low freq power (VRF18 from PMIC)	AVDD18_VRXLF
AVDD18_VRXHF	P	Cell RF RX high freq power (VRF18 from PMIC)	AVDD18_VRXHF
AVDD18_VTXLF	P	Cell RF TX low freq power (VRF18 from PMIC)	AVDD18_VTXLF
AVDD18_VTXHF	P	Cell RF TX high freq power (VRF18 from PMIC)	AVDD18_VTXHF
Digital Power			
DVDD18	P	Digital power input for 1.8V IO	DVDD18
DVDD18_IO1	P	Digital power input for 1.8V IO	DVDD18_IO1
DVDD18_IO2	P	Digital power input for 1.8V IO	DVDD18_IO2
DVDD18_IO5	P	Digital power input for 1.8V IO	DVDD18_IO5
DVDD18_MSDC0	P	Digital power input for MSDC0 IO	DVDD18_MSDC0
DVDD28	P	Digital power input for 2.8V IO	DVDD28
DVDD28_MSDC1	P	Digital power input for MSDC0 IO	DVDD28_MSDC1
VCCIO_EMI	P	Digital power input for EMI IO	VCCIO_EMI
VCCK	P	Core power	VCCK
DVDD10_PROC	P	Processor core power	DVDD10_PROC
FSOURCE_P	P	Efuse power	FSOURCE_P
Analog Ground			
AVSS33_USB	G	Analog ground for USB	AVDD33_USB
AVSS18_ABB	G	Analog ground for USB	AVDD18_AP
DVSS18_MIPIIO	G	Analog ground for MIPI (DSI & CSI0 & CSI1)	DVDD18_MIPIIO

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Ball name	Type	Description	Power domain
DVSS18_MIPITX	G	CellRF RF ground	DVSS18_MIPITX
AVSS_CONN	G	Connectivity ABB ground	AVDD18_WBG
AVSS_CEL	G	CellRF RF ground	
DETGND	G	CellRF TX detection path ground	
Digital Ground			
GND	G	Digital ground	

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-4. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
DVDD10_PROC	Digital power input for processor	-0.15	1.31	V
VCCK	Digital power input for core	-0.15	1.31	V
DVDD18	Digital power input for 1.8V IO	-0.3	2.1	V
DVDD18_IO1	Digital power input for 1.8V IO	-0.3	2.1	V
DVDD18_IO2	Digital power input for 1.8V IO	-0.3	2.1	V
DVDD18_IO5	Digital power input for 1.8V IO	-0.3	2.1	V
DVDD18_MIPIIO	Analog power 1.8V for MIPI	-0.3	1.98	V
DVDD18_MIPITX	Analog power 1.8V for MIPI	-0.3	1.98	V
AVDD18_USB	Analog power 1.8V for USB	-0.3	1.98	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX, RF VIO	-0.3	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0 IO	-0.3	2.1	V
DVDD18_MSDC1	Digital power input for MSDC1 IO	-0.3	2.1	V
AVDD18_AP	Analog power Input 1.8V for AUXADC, TSENSE	-0.3	1.98	V
DVDD28	Digital power input for 2.8V IO	-0.3	3.63	V
DVDD28_MSDC1	Digital power input for MSDC0 IO	-0.3	3.63	V
VCCIO_EMI	Digital power input for EMI IO	-0.3	1.3	V
AVDD28_DAC	Analog power input 2.8V for APC	-0.3	3.08	V
AVDD33_USB	Analog power 3.3V for USB	-0.3	3.63	V
AVDD18_FM	Analog power 1.8V for FM	-0.3	2.1	V
AVDD18_GPS	Analog power 1.8V for GPS	-0.3	2.1	V
AVDD18_WBT_AFE	Analog power 1.8V for WBT AFE	-0.3	2.1	V
AVDD18_WBT	Analog power 1.8V for WBT	-0.3	2.1	V
AVDD33_WBT	Analog power 3.3V for WBT	-0.3	3.6	V
AVDD_VIO18	Analog power 1.8V for Cell RF ISO and LSFLDO (VIO18 from PMIC)	TBD	2.31	V
VXODIG	Cell RF 32k/32kless power domain switch (VIO18 or VTCXO22)	Follow VIO18 or VTCXO22 spec depending on 32k/32kless mode.		
VTCXO22	Cell RF DCXO core/buffer power (VTCXO22 from PMIC)	TBD	4.5	V
AVDD18_VRXLF	Cell RF RX low freq power (VRF18 from PMIC)	TBD	2.31	V
AVDD18_VRXHF	Cell RF RX high freq power (VRF18 from PMIC)	TBD	2.31	V
AVDD18_VTXLF	Cell RF TX low freq power (VRF18 from PMIC)	TBD	2.31	V
AVDD18_VTXHF	Cell RF TX high freq power (VRF18 from PMIC)	TBD	2.31	V

Warning: Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.

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2.2.2 Recommended Operating Conditions

Table 2-5. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD10_PROC	Digital power input for processor	0.85	1.15	1.31	V
VCCK	Digital power input for core	0.85	1.15	1.31	V
DVDD18	Digital power input for 1.8V IO	1.7	1.8	1.9	V
DVDD18_IO1	Digital power input for 1.8V IO	1.7	1.8	1.9	V
DVDD18_IO2	Digital power input for 1.8V IO	1.7	1.8	1.9	V
DVDD18_IO5	Digital power input for 1.8V IO	1.7	1.8	1.9	V
DVDD18_MIPIIO	Analog power 1.8V for MIPI	1.7	1.8	1.9	V
DVDD18_MIPITX	Analog power 1.8V for MIPI	1.7	1.8	1.9	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.8	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX, RF VIO	1.7	1.8	1.9	V
DVDD18_MSDC0	Digital power input for MSDC0 IO	1.7	1.8	1.9	V
DVDD18_MSDC1	Digital power input for MSDC1 IO	1.7	1.8	1.9	V
AVDD18_AP	Analog power Input 1.8V for AUXADC, TSENSE	1.7	1.8	1.9	V
DVDD28	Digital power input for 2.8V IO	2.52	2.8	3.08	V
DVDD28_MSDC1	Digital power input for MSDC0 IO	1.7 2.7	1.8 3.3	1.95 3.6	V
VCCIO_EMI	Digital power input for EMI IO	1.14	1.2	1.3	V
AVDD28_DAC	Analog power input 2.8V for APC	2.6	2.8	3	V
AVDD33_USB	Analog power 3.3V for USB	2.97	3.3	3.63	V
AVDD18_FM	Analog power 1.8V for FM	1.72	1.8	1.98	V
AVDD18_GPS	Analog power 1.8V for GPS	1.72	1.8	1.98	V
AVDD18_WBT_AFE	Analog power 1.8V for WBT AFE	1.72	1.8	1.98	V
AVDD18_WBT	Analog power 1.8V for WBT	1.72	1.8	1.98	V
AVDD33_WBT	Analog power 3.3V for WBT	3.3	3.5	3.6	V
AVDD_VIO18	Analog power 1.8V for Cell RF ISO and LSFLDO (VIO18 from PMIC)	1.725	1.8	1.875	V
VXODIG	Cell RF 32k/32kless power domain switch (VIO18 or VTCXO22)	Follow VIO18 or VTCXO22 spec depending on 32k/32kless mode.			
VTCXO22	Cell RF DCXO core/buffer power (VTCXO22 from PMIC)	2.1	2.2	2.3	V
AVDD18_VRXLF	Cell RF RX low freq power (VRF18 from PMIC)	1.75	1.825	1.9	V
AVDD18_VRXHF	Cell RF RX high freq power (VRF18 from PMIC)	1.75	1.825	1.9	V
AVDD18_VTXLF	Cell RF TX low freq power (VRF18 from PMIC)	1.75	1.825	1.9	V
AVDD18_VTXHF	Cell RF TX high freq power (VRF18 from PMIC)	1.75	1.825	1.9	V

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2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours at factory conditions of 30°C/60% RH, or
   - Stored at 20% RH.
3. Devices require baking before mounting, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH for low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C for high temperature device containers.

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2.3 DRAM Timing Diagram

2.3.1 Introduction

The DRAM speed of MT6580 supports up to LPDDR2-1066 and LPDDR3-1066.The measurement point for all signals follows the definition in JEDEC DRAM standard. Timing symbols in this section match the JEDEC DRAM standard. This section describes the timing characteristics when LPDDR2/LPDDR3 SDRAM are used.

2.3.2 DDRPHY Clock

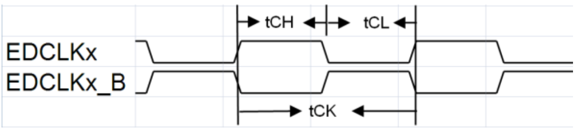

Figure 2-2. DDRPHYclock EDCLKx and EDCLKx_B

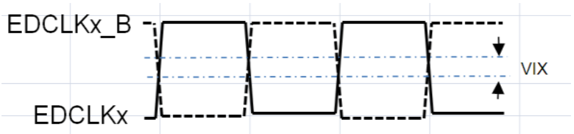

Figure 2-3. Differential signals of DDRPHY clock

Table 2-6. DDRPHYclock timing parameters

Symbol	Parameter	Min.	Max.	Unit
tCK	Clock cycle time	1.875	-	ps
tCH	Clock high-level width	0.45	0.55	tCK
tCL	Clock low-level width	0.45	0.55	tCK
VIX	Differential clock cross point voltage	-120	120	mV

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2.3.3 DRAM Read and Write Timing

2.3.3.1 Read and Write Timing of LPDDR2

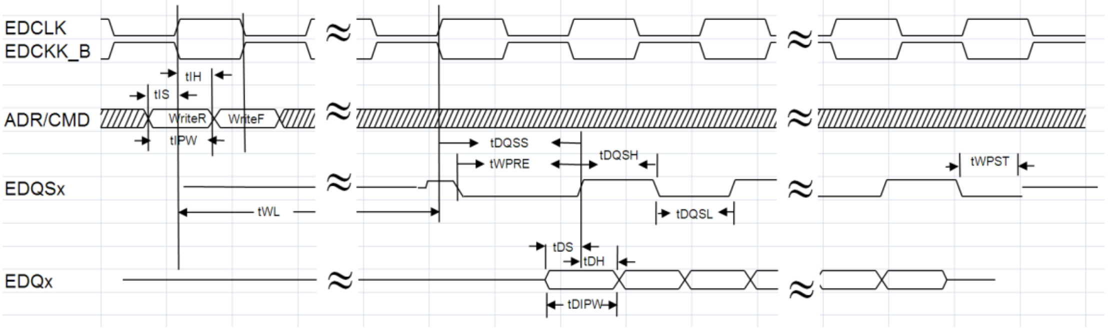

Figure 2-4. LPDDR2 write timing

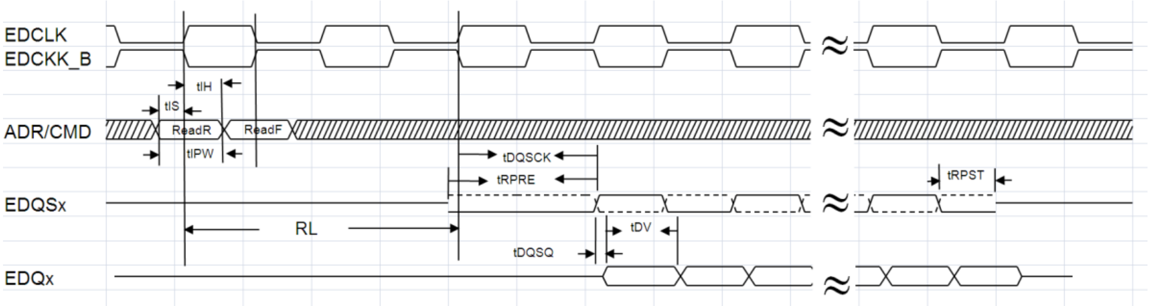

Figure 2-5. LPDDR2 read timing

Table 2-7. LPDDR2 1066 timing parameters

Symbol	Parameter	Min.	Max.	Unit
tIS	Address and control setup input setup time	220	-	ps
tIH	Address and control input hold time	220	-	ps
tIPW	Address and control input pulse width	0.4	-	tCK
Timing of Read Cycle				
tRPRE	Read preamble	0.9	-	tCK
tRPST	Read postamble	0.45	-	tCK
tDQSQ	DQS-DQ skew	-	200	ps
tDQSCK	DQS access time form CK/CK_B	2000	5500	ps
Timing of Write Cycle				
tDQSS	Write command to the 1st DQS latching transition	0.75	1.25	tCK
tWPRE	Write pretamble	0.35	-	tCK
tWPST	Write postamble	0.4	-	tCK
tDS	DQ and DQM setup time	210	-	ps
tDH	DQ and DQM hold time	210	-	ps
tDIPW	DQ and DQM pulse width	0.35	-	tCK
tDQSH	DQS high-level width	0.4	-	tCK

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Symbol	Parameter	Min.	Max.	Unit
tDQSL	DQS low-level width	0.4	-	tCK

2.3.3.2 Read and Write Timing of LPDDR3

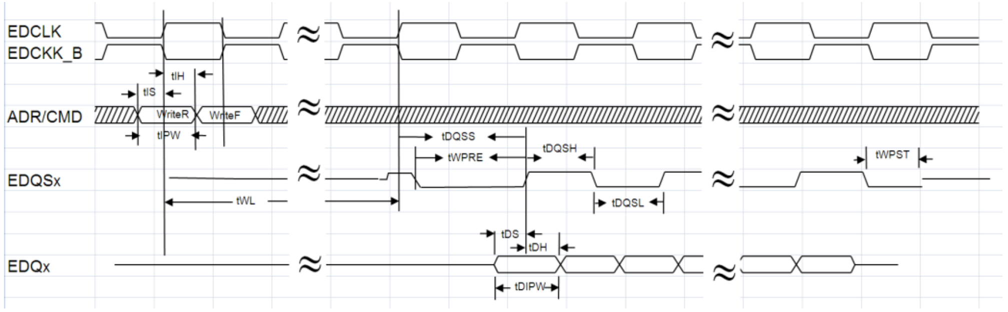

Figure 2-6. LPDDR3 write timing

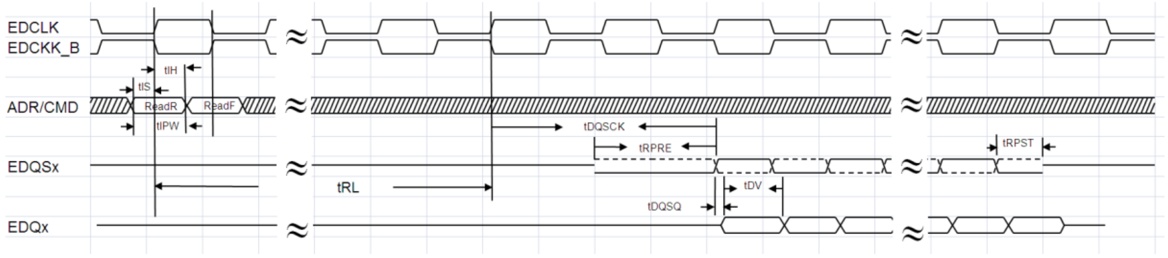

Figure 2-7. LPDDR3 read timing

Table 2-8. LPDDR3 1066 timing parameters

Symbol	Parameter	Min.	Max.	Unit
tIS	Address and control setup input setup time	220	-	ps
tIH	Address and control input hold time	220	-	ps
tIPW	Address and control input pulse width	0.4	-	tCK
Timing of Read Cycle				
tRPRE	Read preamble	0.9	-	tCK
tRPST	Read postamble	0.3	-	tCK
tDQSQ	DQS-DQ skew	-	200	ps
tDQSCK	DQS access time from CK/CK_B	2500	5500	ps
Timing of Write Cycle				
tDQSS	Write command to the 1st DQS latching transition	0.75	1.25	tCK
tWPRE	Write pretamble	0.8	-	tCK
tWPST	Write postamble	0.4	-	tCK
tDS	DQ and DQM setup time	210	-	ps
tDH	DQ and DQM hold time	210	-	ps
tDIPW	DQ and DQM pulse width	0.35	-	tCK
tDQSH	DQS high-level width	0.4	-	tCK

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Symbol	Parameter	Min.	Max.	Unit
tDQSL	DQS low-level width	0.4	-	tCK

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2.4 System Configuration

2.4.1 Mode Selection

Table 2-9. Mode selection

Pin name	Description
[0] PWRAP_SPI0_CSN [1] BPI_BUS10 [2] BPI_BUS11	0xx: Boot from eMMC 100: LPDDR2 SLC NAND 101: LPDDR2 MLC NAND 110: Legacy NAND 111: Toggle/ONFI NAND
KCOL0	0: Force USB download mode in bootrom 1: NA (default)
[0] AUD_CLK_MOSI [1] SIM1_SCLK	00: No dedicate JTAG 01: Use SPI1 pin for JTAG 10: Use MC1 pins for JTAG 11: Use CAM pins for JTAG

2.4.2 Constant Tie Pins

Table 2-10. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.5 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

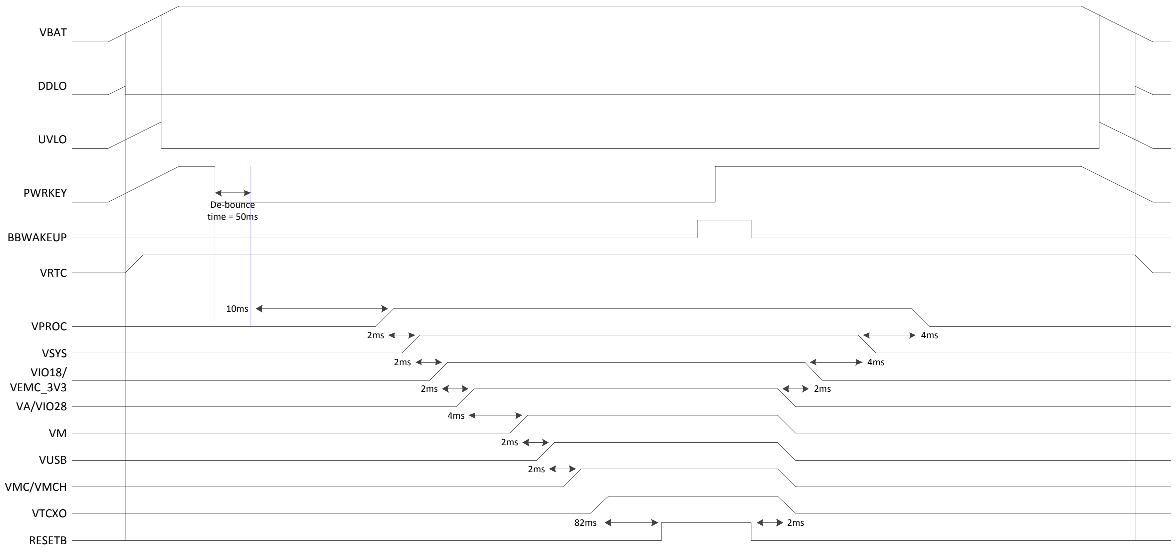

Figure 2-8. Power on/off sequence with XTAL

Note that the above figure only shows one power-on/off condition with XTAL. The external PMIC for application processor handles the power ON and OFF of the handset. The following three different methods switch on the handset (when VBAT ≥ 3.2V):

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- Pulling PWRKEY low (The user presses PWRKEY.)
- Pulling BBWAKEUP high
- Valid charger plug-in

Pulling PWRKEY low is a normal way to turn on the handset, which turns on regulators as long as the PWRKEY is kept low. PMIC outputs reset signal RESETB to application processor SYSRSTB input. After SYSRSTB is de-asserted, the microprocessor starts and pulls BBWAKEUP high. After that PWRKEY can be released. Pulling BBWAKEUP high will also turn on the handset. This is the case when the alarm in the RTC expires.

Besides, applying a valid external supply on CHRIN will also turn on the handset. However, if the battery is in the UV state (VBAT < 3.2V), the handset cannot be turned on in any way.

The UVLO function in PMIC prevents system startup when the initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is bigger than 3.2V, the UVLO comparator switches and threshold are reduced to 2.75V, which allows the handset to start smoothly unless the battery decays to 2.75V and below.

Once PMIC enters the UVLO state, it draws very low quiescent current. The VRTC LDO will still be active until the DDLO disables it.

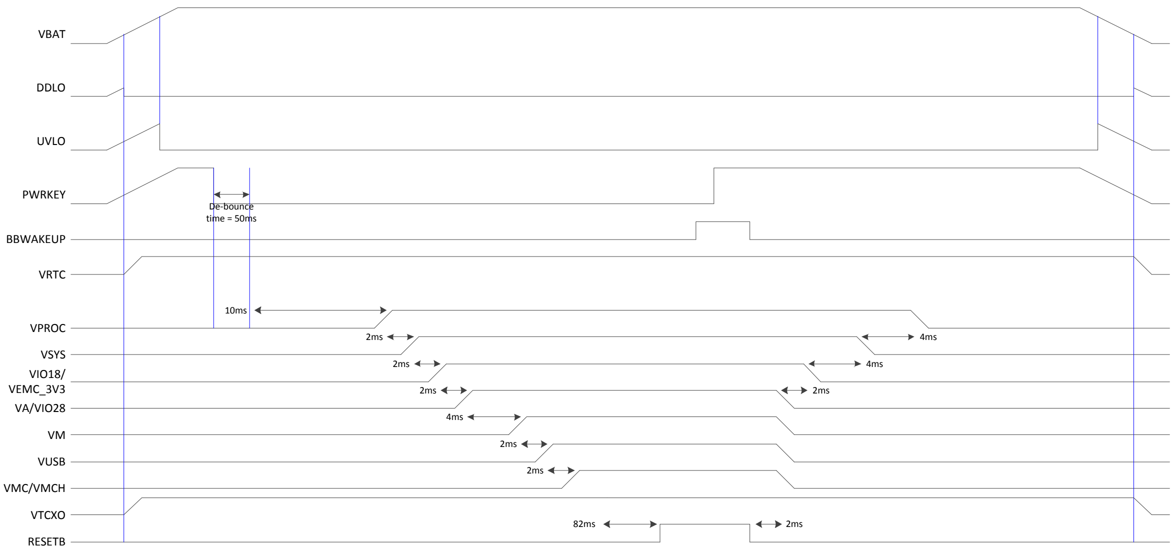

Figure 2-9. Power on/off sequence without XTAL

The figure above shows the power-on/off sequence without XTAL. VTCXO is always turned on when VBAT is above the DDLO threshold.

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2.6 Cellular RF Characteristic

2.6.1 Recommended Operating Conditions

Table 2-11. Recommended operating conditions for cellular RF I/O

Parameter	Conditions	Min.	Typ.	Max.	Unit
Receiver Front End					
RX input frequency range	See section “2.6.4 Receiver” for detailed frequency ranges.				
Rx required amplitude balance	All Rx input pairs	-1		+1	dB
Rx required phase balance	All Rx input pairs	-10		+10	deg
Transmitter					
Tx frequency range	See section “2.6.3 Transmitter” for detailed frequency ranges.				
Tx O/P VSWR	All Phases ZL = 50Ω			2:1	
Clock Buffers					
XO_NFC_TP3, XO_AUD_TP4 load (Rload||Cload) to GND	Cload	See section 2.6.2.1.			pF
	Rload				kΩ
Reference Clock Input					
Reference clock frequency			26.0		MHz
Reference clock input voltage swing	DC coupled at input pin	700		1,500	mVpp
Duty cycle		40		60	%
Phase noise (Note 2)	@ F_{offset} = 100Hz		<-103	-100	dBc/Hz
	@ F_{offset} = 1kHz		<-133	-130	dBc/Hz
	@ F_{offset} = 10kHz		<-147	-144	dBc/Hz
	@ F_{offset} = 100kHz		<-149	-146	dBc/Hz
Harmonic Content	HD2 @ 52MHz			-8	dBc
	HD3 @ 78MHz			-10	dBc
	HD4 @ 104MHz			-20	dBc
Start-up time	|Δf|<1ppm to >90% of final amplitude			3	ms
Crystal Requirements					
2 crystal types are supported (Crystal #1 3225 body size/Crystal #2 2520 body size).					
Nominal load capacitance	Crystal #1		7.5		pF
	Crystal #2		7.0		pF
Initial frequency error				±10	Ppm
ESR				30	Ω
Drive level				100	µW
Pullability	Crystal #1	-10%	32	+10%	ppm/pF
	Crystal #2	-10%	27	+10%	ppm/pF

Note:

1. The supported ambient temperature range depends on the thermal impedance of the package used, the exact operational state and the end application thermal design (housing, PCB, etc.). The junction temperature is a more reliable indication of the actual operational range.
2. The input clock requirement specified is defined to meet receiver and transmitter phase noise requirements, e.g. IC EVM specification. Certain connectivity requirements may require better

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specifications than this. The clock source (non DCXO mode) can be another transceiver clock buffer when considering multiple transceiver applications.

2.6.2 Reference Clock

A 26MHz DCXO with 2 external 26MHz cock buffers (XO_NFC_TP3, XO_AUD_TP4) and one 32kHz clock output is integrated in the MT6580 RF system.

The mode of operation (internal DCXO or external CLK) is selected via the inputs EN_32K_TP1 and XMODE_TP2 with the following function.

Table 2-12. Reference clock operation mode

EN_32K_TP1	XMODE_TP2	Mode
Low	Low	External CLK
High	High	DCXO without RTC
Low	High	DCXO with RTC

2.6.2.1 Reference Output Clock Buffers Specification

Table 2-13. Reference output clock buffer specification

	XO_AUD_TP4	XO_NFC_TP3
Max. driving capability	30pF // 3K	30pF // 3K
Swing Vpp (Max./Min.)	1.2V/0.7V	0.8V/0.3V
Waveform	Square	Sine
PN requirement 5Hz	-73 (worst)	-73 (worst)
PN requirement 10Hz	-80 (worst)	-80 (worst)
PN requirement 100Hz	-105 (worst)	-105 (worst)
PN requirement 1kHz	-127 (worst)	-122 (worst)
PN requirement 10kHz	-140 (worst)	-125 (worst)
PN requirement 100kHz	-143 (worst)	-133 (worst)

2.6.3 Transmitter

2.6.3.1 3G Transmitter Chain Performance

Table 2-14. Cellular RF 3G transmitter chain performance

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
3G Transmitter Output						
Output return loss	S22		-10		dB	50 Ω load

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Max. output power (QPSK)	Pmax		5.9		dBm	B1
Min. output power (QPSK)	Pmin		-72		dBm	B1
Max. output power (16QAM)	Pmax		2.2		dBm	B1
Min. output power (16QAM)	Pmin		-75.5		dBm	B1
ACLR1 (QPSK)			-46		dB	at Pout=0 dBm
ACLR2 (QPSK)			-70		dB	at Pout=0 dBm
RMS EVM (QPSK)			2.5		%	at Pout=0dBm
ACLR1 (16QAM)			-50		dB	at Pout=0dBm
ACLR2 (16QAM)			-68		dB	at Pout=0dBm
RMS EVM (16QAM)			3		%	at Pout=0dBm
Spectrum Emission Mask						
Carrier leakage			-45		dBc	After calibration with BB
Sideband suppression			-45		dBc	After calibration with BB
Noise Emissions						
Band I, noise in RX			-162.0		dBc/Hz	at Pout=0 dBm
Band II, noise in RX			-160.0		dBc/Hz	at Pout=0 dBm
Band V, noise in RX			-161.0		dBc/Hz	at Pout=0 dBm
Band VIII, noise in RX			-161.0		dBc/Hz	at Pout=0 dBm

2.6.3.2 2G Transmitter Chain Performance

Table 2-15. Cellular RF 2G transmitter chain performance

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
2G Transmitter Output						
Output return loss	S_{22}		-10		dB	50 Ω load
Max. output power, LB (GMSK)	P_{max}	1	3	5	dBm	
Max. output power, HB (GMSK)	P_{max}	0.5	2.5	4.5	dBm	
Max. output power, LB (8PSK)	P_{max}	-2			dBm	
Max. output power, HB (8PSK)	P_{max}	0			dBm	
Min. output power (8PSK)	P_{min}		-44		dBm	
ORFS 400k, LB (GMSK)	$ORFS_{400k}$		-69		dBc	
ORFS 400k, HB (GMSK)	$ORFS_{400k}$		-66		dBc	
ORFS 400k, LB (8PSK)	$ORFS_{400k}$		-66		dBc	
ORFS 400k, HB (8PSK)	$ORFS_{400k}$		-65		dBc	
Modulation Accuracy (GMSK)						
RMS phase error, LB	Φ_{RMS}		0.5		deg	
RMS phase error, HB	Φ_{RMS}		1		deg	
PEAK phase error, LB	Φ_{Peak}		2.5		deg	

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PEAK phase error, HB	Φ_{Peak}		4.5		deg	
Modulation Accuracy (8PSK)						
RMS EVM, LB	EVM_{RMS}		1.8		%	
RMS EVM, HB	EVM_{RMS}		2.1		%	
Peak EVM, LB	EVM_{Pk}		8		%	
Peak EVM, HB	EVM_{Pk}		14		%	
Noise Emissions (GMSK)						
20MHz offset, LB			-168		dBc/Hz	
32MHz offset, LB			-170		dBc/Hz	
20MHz offset, HB			-164		dBc/Hz	
32MHz offset, HB			-165		dBc/Hz	
Noise Emissions (8PSK)						
20MHz offset, LB			-157		dBc/Hz	at Pout=-4dBm
32MHz offset, LB			-158		dBc/Hz	
20MHz offset, HB			-156		dBc/Hz	
32MHz offset, HB			-157		dBc/Hz	
Harmonic Emissions						
2nd harmonic			-25		dBc	
3rd harmonic			-10		dBc	
4th harmonic			-25		dBc	

2.6.4 Receiver

2.6.4.1 Celluar RF Receiver Target Specification

2G GSM/GPRS/EDGE

Table 2-16. Cellular RF 2G receiver target specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input return loss	(Note 1)	-10			dB
Input frequency	For all bands	869		1,990	MHz
Voltage gain	Maximum receiver gain		56		dB
3 dB cut-off frequency	2G mode		1.0		MHz
Noise figure	Maximum gain (Note1) (Note2) (Note4)		2.5	3	dB
	With ±3MHz offset blocker (Note 1) (Note 2) (Note 5)		11		dB
	With ±20MHz offset blocker (Note 1) (Note 2) (Note 6)		13		dB
Input IP3	±0.8MHz and ±1.6MHz offset, 2G	-10	-8		dBm
Input IP2	±6MHz offset, 2G	35	45		dBm
Current consumption	From 1.5 V supply, maximum gain, high band (Note 3)		63		mA

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Parameter	Conditions	Min.	Typ.	Max.	Unit
	From 1.5 V supply, maximum gain, low band (Note 3)		58		mA

3G WCDMA

Table 2-17. Cellular RF 3G WCDMA receiver target specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input return loss	(Note 1)	-10			dB
Input frequency	For all bands	869		2170	MHz
Voltage gain	Maximum receiver gain		60		dB
3 dB cut-off frequency	3G WCDMA mode		3.6		MHz
Noise figure	Maximum gain (Note 1) (Note 4) (Note 7)		2.5	3	dB
Input IP3	±10MHz and ±20MHz offset; low band	-9	-7		dBm
	±3.5MHz and ±5.9MHz offset mid gain	-2	0		dBm
	±3.5MHz and ±6.5MHz offset, max gain	-10	-8		dBm
	±3.5MHz and ±6.5MHz offset, mid gain	-2	0		dBm
	±3.5MHz and ±6.5MHz offset, low gain	8	11		dBm
	-80MHz and -160MHz offset	-7	-5		dBm
	-45MHz and -90MHz offset	-7	-5		dBm
Input IP2	Tx offset	45	60		dBm
	±4.5MHz and ±5.5MHz offset, low gain	40	50		dBm
	±14.5MHz and ±15.5MHz offset, max gain	35	45		dBm
Current consumption	From 1.5 V supply, maximum gain, high band (Note 3)		41		mA
	From 1.5 V supply, maximum gain, low band (Note 3)		37		mA

Note:

1. Source/reference impedance: 50Ω, with balun or single-to-differential SAW filter and matching network
2. Noise averaged over GGE channel
3. Includes RX LDO, LNA, SRX, LO divide-by-2 (or divide-by-4), 25% duty-cycle generation and buffers, and analog baseband filter
4. No blockers
5. Blocker power is 4dB larger than standard spec.
6. Blocker power is 3dB larger than standard spec.
7. Noise averaged over WCDMA channel

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2.7 Connectivity RF Characteristic

2.7.1 Wi-Fi RF Radio Characteristic

The WLAN radio characteristics are described in this section. Unless otherwise specified, all specifications are measured at the chip output bumps.

2.7.1.1 Wi-Fi Receiver Specification

Note: The specification value is valid at room temperature (25°C).

Table 2-18. 2.4GHz receiver specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,412	-	2,484	MHz
RX sensitivity [a]	1 Mbps DSSS		-98		dBm
	2 Mbps DSSS		-95		dBm
	5.5 Mbps DSSS		-93		dBm
	11 Mbps DSSS		-90		dBm
RX Sensitivity [a]	6 Mbps OFDM		-95		dBm
	9 Mbps OFDM		-93		dBm
	12 Mbps OFDM		-92		dBm
	18 Mbps OFDM		-89.5		dBm
	24 Mbps OFDM		-86.5		dBm
	36 Mbps OFDM		-83		dBm
	48 Mbps OFDM		-79		dBm
	54 Mbps OFDM		-77.5		dBm
RX sensitivity [b]	MCS 0		-94.5		dBm
BW = 20MHz	MCS 1		-91.5		dBm
Green field	MCS 2		-89		dBm
800nS guard interval	MCS 3		-86		dBm
Non-STBC	MCS 4		-82.5		dBm
	MCS 5		-78		dBm
	MCS 6		-76.5		dBm
	MCS 7		-75.5		dBm
RX sensitivity	MCS 0		-91.5		dBm
BW = 40MHz	MCS 1		-88.5		dBm
Green field	MCS 2		-86		dBm
800nS guard interval	MCS 3		-82.5		dBm
Non-STBC	MCS 4		-79.5		dBm
	MCS 5		-75		dBm
	MCS 6		-73.5		dBm
	MCS 7		-72.5		dBm
Maximum receive level	11 Mbps DSSS			-5	dBm

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Parameter	Description	Min.	Typ.	Max.	Unit
	6 Mbps OFDM			-10	dBm
	54 Mbps OFDM			-10	dBm
	MCS0			-10	dBm
	MCS7			-10	dBm
Adjacent channel rejection (30MHz offset)	1 Mbps DSSS		40	40	dB
Adjacent channel rejection (25MHz offset)	11 Mbps DSSS		40	40	dB
Adjacent channel rejection (25MHz offset)	6 Mbps OFDM		34		dB
	54 Mbps OFDM		22		dB
Adjacent channel rejection (25MHz offset), BW = 20MHz	MCS 0		25		dB
	MCS 7		5		dB
Adjacent channel rejection (40MHz offset), BW = 40MHz	MCS 0		26		dB
	MCS 7		1		dB
Blocking level for 1dB RX sensitivity degradation	776 ~ 794 MHz CDMA2000		TBD		dBm
	824 ~ 849 MHz GSM		TBD		dBm
	880 ~ 915 MHz GSM		TBD		dBm
	1,710 ~ 1,785 MHz GSM		TBD		dBm
	1,850 ~ 1,910 MHz GSM		TBD		dBm
	1,850 ~ 1,910 MHz WCDMA		TBD		dBm
	1,920 ~ 1,980 MHz WCDMA		TBD		dBm

a: Degraded by 1.5dB at 85°C
b: Sensitivity degradation in different MCS modes: mixed-mode normal GI: 1dB, mixed-mode short GI: 1dB, and STBC:1dB

2.7.1.2 Wi-Fi Transmitter Specification

Note:
1. The specification value is valid at room temperature (25°C).
2. All specifications are measured at the RF port unless otherwise specified.
3. Typical output power degradation around 3dB at FCC band edge channels

Table 2-19. 2.4GHz transmitter specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,412	-	2,484	MHz
Output power	802.11b, 1~11 Mbps DSSS		22		dBm
VBAT = 3.6V	802.11g, 6 ~54Mbps OFDM		20		dBm
	802.11n, HT20 MCS0~7		18.5		dBm
	802.11n, HT40 MCS0~7		17.5		dBm
EVM	802.11b, 1~11 Mbps DSSS @Pout=22dBm		25		%
	802.11g, 6 ~54Mbps OFDM		-28		dB

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Parameter	Description	Min.	Typ.	Max.	Unit
	@Pout=20dBm				
	802.11n, HT20 MCS0~7 @Pout=18.5dBm		-30		dB
	802.11n, HT40 MCS0~7 @Pout=17.5dBm		-30		dB
TX power accuracy	-40~85 ºC,5~22dBm			±1.5	dB
Loadpull variation at VSWR = 2:1	Output power variation			±1.5	dB
	EVM degradation		4		dB
Transmitted power (Data rate = 6M, Pout = 20dBm)	76 ~ 108 MHz		-142		dBm/Hz
	776 ~ 794 MHz		-142		dBm/Hz
	869 ~ 960 MHz		-142		dBm/Hz
	925 ~ 960 MHz		-142		dBm/Hz
	1,570 ~ 1,580 MHz		-140		dBm/Hz
	1,805 ~ 1,880 MHz		-131		dBm/Hz
	1,930 ~ 1,990 MHz		-126		dBm/Hz
	2,110 ~ 2,170MHz		-125		dBm/Hz
Harmonic output power (Data rate = 1M, Pout = 23dBm) [i]	2nd harmonic			-50	dBm/MHz
	3rd harmonic			-50	dBm/MHz

2.7.2 Bluetooth RF Radio Characteristic

2.7.2.1 Basic Data Rate Receiver Specification

Table 2-20. Basic data rate receiver specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402		2,480	MHz
Receiver sensitivity	BER < 0.1%		-94		dBm
Max. usable signal	BER < 0.1%	-20	-5		dBm
C/I co-channel	Co-channel selectivity (BER < 0.1%)	-	6	11	dB
C/I 1MHz	Adjacent channel selectivity (BER < 0.1%)	-	-7	0	dB
C/I 2MHz	2nd adjacent channel selectivity (BER < 0.1%)	-	-40	-30	dB
C/I ≧3MHz	3rd adjacent channel selectivity (BER < 0.1%)	-	-43	-40	dB
C/I image channel	Image channel selectivity (BER < 0.1%)	-	-20	-9	dB
C/I image 1MHz	1MHz adjacent to image channel selectivity (BER < 0.1%)	-	-35	-20	dB
Out-of-band blocking*	30MHz to 2,000MHz	-4			dBm
	2,001MHz to 2,339MHz	-18			dBm
	2,501MHz to 3,000MHz	-18			dBm
	3,001MHz to 12.75GHz	1			dBm

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Parameter	Description	Min.	Typ.	Max.	Unit
Intermodulation	Max. interference level to maintain 0.1% BER	-30			dBm

2.7.2.1 Basic Data Rate Transmitter Specification

Table 2-21. Basic data rate transmitter specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Output power	At max power output level		12		dBm
Power control step		2	4	8	dB
ICFT	Initial carrier frequency drift	-75	±18	75	kHz
Carrier frequency drift	One slot packet (DH1)	-25	±10	25	kHz
	Three slot packet (DH3)	-40	±10	40	kHz
	Five slot packet (DH5)	-40	±10	40	kHz
	Max. drift rate	-	200	400	Hz/us
Modulation characteristic	$\triangle f1_{avg}$	140	156	175	kHz
	$\triangle f2_{max}$ (for at least 99% of all $\triangle f2_{max}$)	115	145	-	kHz
	$\triangle f2_{avg}/\triangle f1_{avg}$	0.8	0.98	-	
20-dB bandwidth		-	922	1,000	kHz
In-band spurious emission	±2MHz offset		-38	-20	dBm
	±3MHz offset		-43	-40	dBm
	>±3MHz offset		-45		dBm
Out-of-band spurious emission**	30MHz to 1GHz			-64	dBm
	1GHz to 12.75GHz			-50	dBm
	1.8GHz to 1.9GHz			-50	dBm
	5.15 to 5.3GHz			-50	dBm

2.7.2.2 Enhanced Data Rate Receiver Specification

Table 2-22. Enhanced data rate receiver specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Receiver sensitivity	π/4 DQPSK (BER < 0.01%)	-	-95	-70	dBm
	8PSK (BER < 0.01%)	-	-89	-70	dBm
Max. usable signal	π/4 DQPSK (BER < 0.1%)	-20	-5	-	dBm
	8PSK (BER < 0.1%)	-20	-5	-	dBm
C/I co-channel	π/4 DQPSK (BER < 0.1%)	-	9	13	dB
	8PSK (BER < 0.1%)	-	16	21	dB
C/I 1MHz	π/4 DQPSK (BER < 0.1%)	-	-12	0	dB
	8PSK (BER < 0.1%)	-	-6	5	dB

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Parameter	Description	Min.	Typ.	Max.	Unit
C/I 2MHz	π/4 DQPSK (BER < 0.1%)	-	-40	-30	dB
	8PSK (BER < 0.1%)	-	-36	-25	dB
C/I ≧3MHz	π/4 DQPSK (BER < 0.1%)	-	-43	-40	dB
	8PSK (BER < 0.1%)	-	-40	-33	dB
C/I image channel	π/4 DQPSK (BER < 0.1%)	-	-20	-7	dB
	8PSK (BER < 0.1%)	-	-15	0	dB
C/I image 1MHz	π/4 DQPSK (BER < 0.1%)	-	-40	-20	dB
	8PSK (BER < 0.1%)	-	-30	-13	dB

2.7.2.3 Enhanced Data Rate Transmitter Specification

Table 2-23. Enhanced data rate transmitter specification

Parameter	Description		Min.	Typ.	Max.	Unit
Frequency range			2,402		2,480	MHz
Output power	π/4 DQPSK			9		dBm
	8PSK			9		dBm
Relative transmit power	π/4 DQPSK		-4	-1.7	1	dB
	8PSK		-4	-1.7	1	dB
Frequency stability	ω_o	π/4 DQPSK	-10	±4	10	kHz
		8PSK	-10	±4	10	kHz
	ω_i	π/4 DQPSK	-75	±18	75	kHz
		8PSK	-75	±18	75	kHz
	$\lvert\omega_o+\omega_i\rvert$	π/4 DQPSK	-75	±20	75	kHz
		8PSK	-75	±20	75	kHz
Modulation accuracy	RMS DEVM	π/4 DQPSK	-	8	20	%
		8PSK	-	8	13	%
	99% DEVM	π/4 DQPSK	-	11	30	%
		8PSK	-	11	20	%
	Peak DEVM	π/4 DQPSK	-	15	35	%
		8PSK	-	15	25	%
In-band spurious emission	±1MHz offset	π/4 DQPSK		-29		dB
		8PSK		-29		dB
	±2MHz offset	π/4 DQPSK		-23		dBm
		8PSK		-23		dBm
	±3MHz offset	π/4 DQPSK		-40		dBm
		8PSK		-40		dBm

2.7.2.4 LE Receiver Specification

Table 2-24. Bluetooth LE receiver specification

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Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402		2,480	MHz
Receiver sensitivity (*)	PER < 30.8%		-98	-70	dBm
Max. usable signal	PER < 30.8%	-10	-5		dBm
C/I co-channel	Co-channel selectivity (PER < 30.8%)		6	21	dB
C/I 1MHz	Adjacent channel selectivity (PER < 30.8%)		-7	15	dB
C/I 2MHz	2nd adjacent channel selectivity		-30	-17	dB
	(PER < 30.8%)				
C/I ≧3MHz	3rd adjacent channel selectivity		-33	-27	dB
	(PER < 30.8%)				
C/I Image channel	Image channel selectivity (PER < 30.8%)		-20	-9	dB
C/I Image 1MHz	1MHz adjacent to image channel selectivity		-30	-15	dB
	(PER < 30.8%)				
Out-of-band blocking	30MHz to 2,000MHz			-30	dBm
	2,001MHz to 2,339MHz			-35	dBm
	2,501MHz to 3,000MHz			-35	dBm
	3,001MHz to 12.75GHz			-30	dBm

2.7.2.5 LE transmitter specification

Table 2-25. Bluetooth LE transmitter specification

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Output power(*)	At max. power output level	-20	3	10	dBm
Carrier frequency offset and drift	Frequency offset	-150	±10	150	kHz
	Frequency drift	-50	±10	50	kHz
	Max. drift rate	-20	±10	20	Hz/us
Modulation characteristic	$\triangle f1_{avg}$	225	251	275	kHz
	$\triangle f2_{max}$ (For at least 99% of all $\triangle f2_{max}$)	185	215		kHz
	$\triangle f2_{avg}/\triangle f1_{avg}$	0.8	0.88		
In-band spurious emission	±2M offset		-35	-20	dBm
	>±3MHz offset		-40	-30	dBm

*The measurement does not include exceptions in these bands. Exceptions can pass Bluetooth SIG spec.
**The measurement is at chip output.

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2.7.3 GPS RF Radio characteristic

2.7.3.1 GPS receiver specification

Table 2-26. GPS receiver performance

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Horizontal position accuracy (a)	Without aid		3		Meter
	DGPS		2.5		Meter
Velocity accuracy	Without aid		0.1		Meter/Sec
	DGPS		0.05		Meter/Sec
Sensitivity	Autonomous acquisition		-148		dBm
	Warm acquisition		-151		dBm
	Hot acquisition		-163		dBm
	Tracking		-165		dBm
Time To First Fix (b)	Cold start: Autonomous		< 35		Sec
	Warm start: Autonomous		< 34		Sec
	Hot start: Autonomous		<1		Sec
Time To First Fix (b)	MS based: GSM coarse time		< 20		Sec
	MA based: GSM coarse time		< 20		Sec

(a) 2D RMS
(b) Signal power = -130dBm, Fu 0.5 ppm, Tu ±2s, Pu 30km

2.7.4 FM RF Radio Characteristic

2.7.4.1 FM Receiver Specification

Unless otherwise stated, all receiver characteristics are applicable to both long and short antenna ports when operated under the recommended operating conditions. Typical specifications are for channel 98MHz, default register settings and under recommended operating conditions. The minimum and maximum specifications are for extreme operating voltage and temperature conditions, unless otherwise stated.

Table 2-27. FM receiver specification

Description	Condition	Min.	Typ.	Max.	Unit
Input frequency range		65		108	MHz
Sensitivity (long antenna)1,3	SINAD= 26dB, unmatched		3		dB Vemf
	SINAD= 26dB, matched		2		dB Vemf
RDS sensitivity (long antenna)	f = 2kHz, BLER < 5%, unmatched		18		dB Vemf
Sensitivity (short antenna)1,3	SINAD= 26dB, unmatched		3		dB Vemf
RDS sensitivity (short antenna)	f = 2kHz, BLER < 5%, unmatched		18		dB Vemf
LNA input resistance4	Antenna port		2.4k		Ohm

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Description	Condition	Min.	Typ.	Max.	Unit
LNA input capacitance4	Antenna port		8		pF
AM suppression1,4	m = 0.3		58		dB
Adjacent channel selectivity1,4	200kHz		53		dB
Alternate channel selectivity1,4	400kHz		65		dB
Spurious response rejection4	In-band		55		dB
Maximum input level			117		dB Vemf
Audio mono SINAD1,3,4			60		dB
Audio stereo SINAD2,3,4			52		dB
Audio stereo separation4	f = 75kHz		45		dB
Audio output load resistance	Single-ended at AFR/AFL outputs		10k		Ohm
Audio output load capacitance	Single-ended at AFR/AFL outputs		12.5		pF
Audio output voltage1,4	At AFR/AFL outputs		80		mVrms
Audio output THD1,4			0.05	0.1	%
Audio output frequency range	3dB corner frequency	30		15k	Hz
[1] f = 22.5kHz, fm = 1kHz, mono, L = R					
[2] f = 22.5kHz, fm = 1kHz, 50μs de-emphasis, stereo					
[3] A-weighting, BW = 300Hz to 15kHz					
[4] Vin = 60dB Vemf					
[5] Reference clock accuracy assumes ideal FM source. If the input FM source has less frequency error, we recommend you use a reference clock of accuracy within 100ppm so as not to affect the quality of channel scan.					

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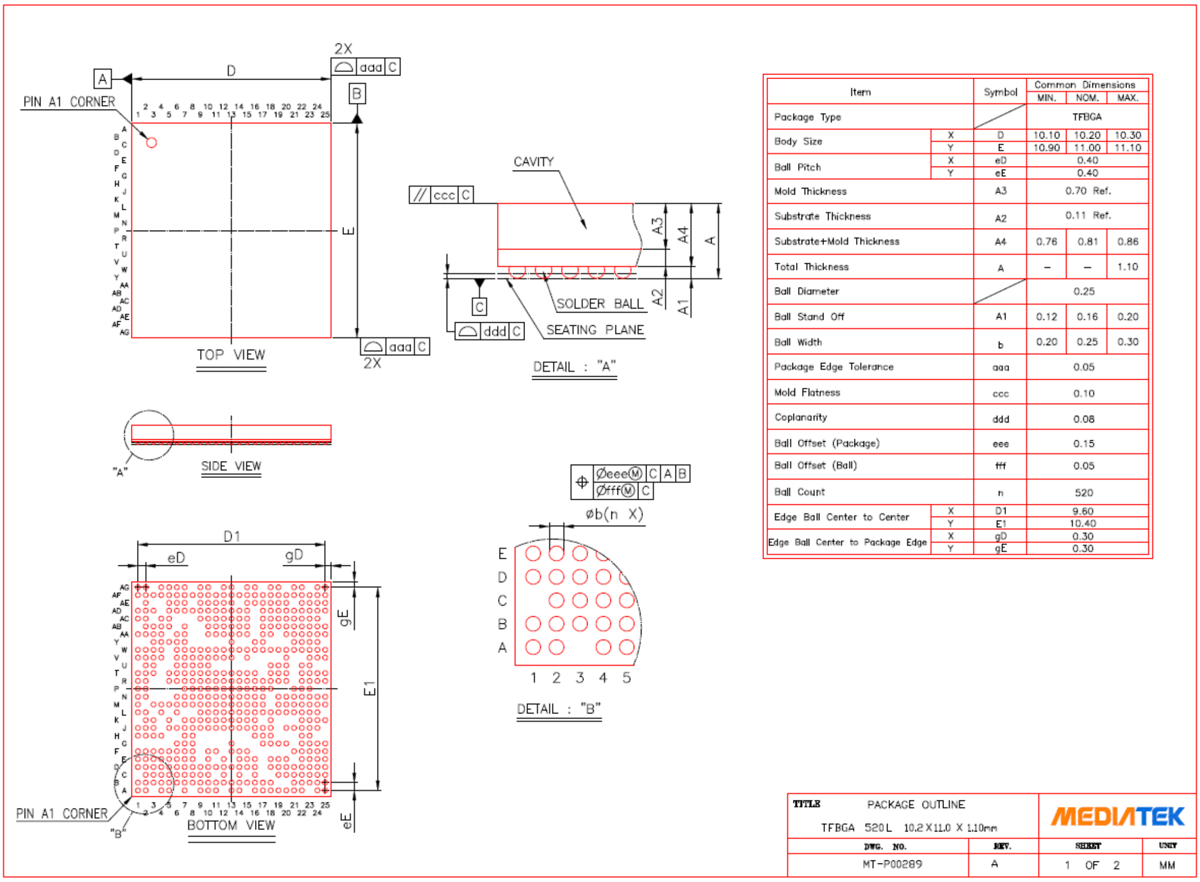
2.8 Package Information

2.8.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			TFBGA		
Body Size	X	D	10.10	10.20	10.30
	Y	E	10.90	11.00	11.10
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.70 Ref.		
Substrate Thickness		A2	0.11 Ref.		
Substrate+Mold Thickness		A4	0.76	0.81	0.86
Total Thickness		A	–	–	1.10
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	520		
Edge Ball Center to Center	X	D1	9.60		
	Y	E1	10.40		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

Figure 2-10. Outlines and dimensions of TFBGA 10.2mm*11.0mm, 520-ball, 0.4mm pitch package

2.8.2 Thermal Operating Specifications

Table 2-28. Thermal operating specifications

Symbol	Description	Value	Unit	Note
Tjunc	Maximum operating junction temperature	125	^{o}C	
Theta JA	Package thermal resistance in nature convection (junction to ambient)	37.5	^{o}C/Watt	
Theta JC	Package thermal resistance in nature convection (junction to case)	8.8	^{o}C/Watt	
Theta JB	Package thermal resistance in nature convection (junction to board)	8.2	^{o}C/Watt	

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2.8.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

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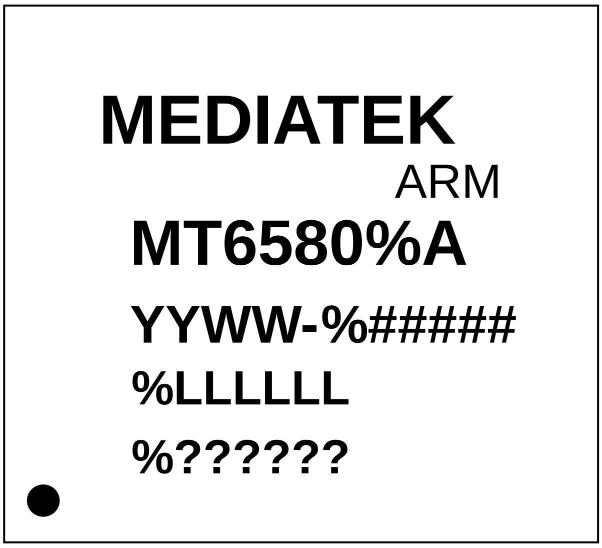
2.9 Ordering Information

2.9.1 Top Marking Definition



- %: Function code
- YYWW: Date code
- #####: Subcontractor code
- LLLLLL: U1 die lot ID
- ?????? : U2 die lot ID

Figure 2-11. Top mark of MT6580

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